File 348:EUROPEAN PATENTS 1978-2005/Nov W01
(c) 2005 European Patent Office
File 349:PCT FULLTEXT 1979-2005/UB=20051110,UT=20051103
(c) 2005 WIPO/Univentio

| Set | Items | Description |
|---|---|---|
| S1 | 48878 | TRISILICON TETRANITRIDE OR SILICON NITRIDE OR SIN OR SILICONITRIDE OR SI()NITRIDE OR SI3N4 |
| S2 | 69636 | TRISILICON()TETRANITRIDE OR SILICON()NITRIDE OR SIN OR SILICONITRIDE OR SI()NITRIDE OR SI3N4 |
| S3 | 240133 | SILICONDIOXIDE OR SILICON()DIOXIDE OR SILICON()OXIDE OR SILICA OR SIO OR SIO2 |
| S4 | 1170986 | VIA? ? OR STUD? ? OR PLUG? ? OR HOLE? ? OR APERTURE? ? OR -RIE OR REACTIVE()ION()ETCH??????? OR THROUGH()HOLE? ? OR SPUTTER???? OR RECESS???? |
| S5 | 197564 | PHOTO(A)(RESIST?????? OR MASK?????? OR LITHOG??????? OR ENGRAV??????) OR PHOTORESIST????? OR PHOTOMASK????????? OR PHOTOLITHO?????? OR PHOTOENGRAV????? OR MASK????? OR LITHOG?????? OR ENGRAV?????? OR ETCH? OR BOE |
| S6 | 237155 | OXIDAT?????? OR LOCOS OR OXIDI????? OR OXIDIZ????? |
| S7 | 567220 | (BOTH OR MULTIPLE? ? OR BACK OR UNDER OR DOUBLE??? OR TWO -OR 2 OR DUPLICAT???? OR FIRST OR SECOND)(2W)(SIDE??? OR SURFACE??? OR SUBSTRATE? ? OR LAYER? ?) OR UNDERSIDE??? OR UNDERETCH??? OR BACKSIDE OR BOTTOM()UP |
| S8 | 40709 | S4(5N)S7 |
| S9 | 969 | S1(5N)S5 |
| S10 | 5023 | S2(5N)(S5 OR S6) |
| S11 | 231 | S8 AND S9 AND S10 |
| S12 | 209 | S11 AND S3 |
| S13 | 35 | S12/TI,AB,CL |
| S14 | 109 | S12/TI,AB,CM |
| S15 | 1247 | IC=(B81B-007/00 OR B81C-001/00 OR H01L-021/78) |
| S16 | 1 | S14 AND S15 |
| S17 | 2 | S15 AND S12 |
| S18 | 1 | S17 NOT S16 |
| S19 | 23 | S1 AND S2 AND S3 AND S4 AND S5 AND S6 AND S7 AND S15 |
| S20 | 22 | S19 NOT S17 |
| S21 | 108 | S14 NOT S19 |
| S22 | 1806 | (CAP???? OR GLASS??)()(DIE? ? OR WAFER? ?) |
| S23 | 4 | S21 AND S22 |
| S24 | 16857 | PACKAG??????(5N)(CHIP? ? OR MICROCHIP? ? OR WAFER? ? OR IC OR INTEGRAT????()CIRCUIT? ? OR TRANSISTOR? ? OR SEMICONDUCT??-???) |
| S25 | 12 | S21 AND S24 |
| S26 | 12 | S25 NOT S23 |
| S27 | 222231 | (MATING OR MATE OR MALE(N)FEMALE OR STACK?????) |
| S28 | 38 | S21 AND S27 |
| S29 | 32 | S28 NOT (S26 OR S19) |

20/5/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS


01656665
Method of fabrication of a microfluidic device
Verfahren zur Herstellung eines mikrofluidischen Bauteiles
Methode de fabrication d'un dispositif microfluidique
PATENT ASSIGNEE:
Micronit Microfluidics B.V., (4119200), Hengelosestraat 705, 7521 PA Enschede, (NL), (Applicant designated States: all)
INVENTOR:
Schlautmann, Stefan, Hoge Bothofstraat 68b, 7511 ZC Enschede, (NL)
Gardeniers, Johannes Gerardus Elisabeth, Timorstraat 6, 7556 SH Hengelo, (NL)
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LEGAL REPRESENTATIVE:
Van Someren, Petronella F. H. M. et al (74791), Arnold & Siedsma, Advocaten en Octrooigemachtigden, Sweelinckplein 1, 2517 GK Den Haag, (NL)
PATENT (CC, No, Kind, Date): EP 1362827 A1 031119 (Basic)
APPLICATION (CC, No, Date): EP 2002076937 020516;
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: B81B-001/00; B81C-001/00

ABSTRACT EP 1362827 A1
The present invention relates to a method of fabricating a microfluidic device including at least two substrates provided with a fluid channel, comprising the steps of:
a) etching at least a channel and one or more fluid ports in a first and/or a second substrate;
b) depositing a first layer on a surface of the second substrate;
c) partially removing the first layer in accordance with a predefined geometry;
d) depositing a second layer on top of the first layer and the substrate surface;
e) planarizing the second layer so as to smooth the upper surface thereof;
f) aligning the first and second substrate;
g) bonding the first substrate on the planarized second layer of the second substrate.
ABSTRACT WORD COUNT: 126

20/5/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS


01640442
Semiconductor device comprising a flexible region and method for manufacturing the same
Halbleitervorrichtung mit flexiblem Bereich und Herstellungsverfahren
Dispositif semi-conducteur comprenant une region flexible, et procede de fabrication associe
PATENT ASSIGNEE:
Sharp Kabushiki Kaisha, (260715), 22-22, Nagaike-cho, Abeno-ku, Osaka-shi, Osaka 545-8522, (JP), (Applicant designated States: all)
INVENTOR:
Tokushige, Nobuaki, 1-9-206, Tsunofurishinya-cho, Nara-shi, Nara 630-8223, (JP)
LEGAL REPRESENTATIVE:
Muller - Hoffmann & Partner (101521), Patentanwalte, Innere Wiener Strasse 17, 81667 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 1351292 A2 031008 (Basic)
EP 1351292 A3 040421
APPLICATION (CC, No, Date): EP 2003007696 030403;
PRIORITY (CC, No, Date): JP 2002104374 020405
DESIGNATED STATES: DE; FR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK
INTERNATIONAL PATENT CLASS: H01L-021/78; H01L-021/762; H01L-029/786; H01L-051/20; G02F-001/1333

ABSTRACT EP 1351292 A2
A semiconductor device comprising a semiconductor layer and one, or a plurality of, semiconductor elements formed on a surface of the semiconductor layer, characterized in that said semiconductor layer is divided into a plurality of pieces in a region wherein said semiconductor layer does not have a semiconductor element and in that the respective pieces of the divided semiconductor layer have a flexible region made of an insulating layer adhered to the sides of the respective pieces so that the pieces are integrated.
ABSTRACT WORD COUNT: 84

20/5/16 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT


01036762 **Image available**
MICROENGINEERED ELECTRICAL CONNECTORS
CONNECTEURS ELECTRIQUES FABRIQUES PAR LA TECHNOLOGIE MEMS
Patent Applicant/Assignee:
MICROSAIC SYSTEMS LIMITED, Department of Electrical and Electronic Engineering, Imperial College, Exhibition Road, London SW7 2BT, GB, GB (Residence), GB (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
SYMS Richard, 59 Woodstock Avenue, London W13 9UQ, GB, GB (Residence), GB (Nationality), (Designated only for: US)
Legal Representative:
MOORE Barry (et al) (agent), Hanna Moore & Curley, 135 Westhall Road, Warlingham, Surrey CR6 9HJ, GB,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200366515 A2-A3 20030814 (WO 0366515)
Application: WO 2003GB314 20030127 (PCT/WO GB0300314)
Priority Application: GB 20023047 20020208

Main International Patent Class: B81C-001/00
International Patent Class: B81C-003/00; B81B-007/00; H01R-043/00
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 7339

English Abstract
A miniature, multi-element electrical connector fabricated using micro-electro-mechanical systems technology is described. Shaped elastic cantilever elements (12) are formed on the female part (11) by deposition of conducting material on a surface that has been previously shaped to define a localised contact area and a sloped entrance face. The cantilevers (12) are then undercut. A similar process is used to construct a sloping face on the male part (10) for easy insertion. An etching process is used to fabricate an interlocking alignment system (20, 21, 22) on the two parts. Erosion of a convex corner is used to form a tapered entrance (22) to this alignment system.

20/5/20 (Item 7 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT


00988093 **Image available**
MEMS AND METHOD OF MANUFACTURING MEMS
MEMS ET PROCEDE DE PRODUCTION DE MEMS
Patent Applicant/Assignee:
REVEO INC, 85 Executive Boulevard, Elmsford, Ny New York 10523, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
FARIS Sadeg M, 24 Pocantico Road, Pleasantville, NY 10570, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
CRISPINO Ralph J (agent), Reveo, Inc., 85 Executive Boulevard, Elmsford, NY 10523, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200316205 A2-A3 20030227 (WO 0316205)
Application: WO 2002US26090 20020815 (PCT/WO US02026090)
Priority Application: US 2001312659 20010815

Main International Patent Class: B81C-001/00
International Patent Class: B81C-005/00; H01L-021/78
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 12340

English Abstract
The present invention relates to micro electro-mechanical systems (MEMS) and production methods thereof, and more particularly to vertically integrated MEMS systems. Manufacturing of MEMS and vertically integrated MEMS is facilitated by forming, preferably on a wafer level, plural MEMS on a MEMS layer selectively bonded to a substrate, and removing the MEMS layer intact.

26/5/12 (Item 5 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT


00183345
FABRICATING ELECTRONIC CIRCUITRY UNIT CONTAINING STACKED IC LAYERS HAVING LEAD REROUTING
PRODUCTION D'UNITES DE CIRCUITS ELECTRONIQUES CONTENANT DES COUCHES EMPILEES DE CIRCUITS INTEGRES A REACHEMINEMENT DES CONDUCTEURS
Patent Applicant/Assignee:
IRVINE SENSORS CORPORATION,
Inventor(s):
GO Tiang C +di,
MINIHAN Joseph A,
SHANKEN Stuart N,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9100683 A2 19910124
Application: WO 90US3705 19900628 (PCT/WO US9003705)
Priority Application: US 89241 19890707
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AT BE CH DE DK ES FR GB IT JP LU NL SE
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 8173

English Abstract
A process and product are disclosed which apply advanced concepts of Z-technology to the field of dense electronic packages. Starting with standard chip-containing silicon wafers (fig. 1, 20), modification procedures are followed which create IC chips (fig. 4, 38) having rerouted gold leads (fig. 4, 30) on top of passivation (fig. 6, 52) (which covers the original silicon (fig. 6, 48) and its aluminum or other metallization (fig. 6, 44)). The modified chips (fig. 4, 38) are cut from the wafers (fig. 1, 20), and then stacked to form multi-layer IC devices (fig. 10b, 60). A stack has one or more access planes (fig. 10c, 64). After stacking, and before applying gold metallization on the access plane, a selective etching step removes any aluminum (or other material) which might interfere with the gold metallization formed on the access planes (figs. 11 and 12). Gold terminal pads (fig. 15, 92) are formed in contact with the terminals of the gold rerouting leads (fig. 15, 66) on the stacked chips, thereby forming gold-to-gold T-connections (fig. 14) for maximum conducting efficiency.

23/5/4 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT


00519553 **Image available**
WAFER-PAIR HAVING DEPOSITED LAYER SEALED CHAMBERS
PAIRE DE TRANCHES FORMANT DES CAVITES HERMETIQUES COMBLEES PAR DEPOT D'UNE COUCHE

Patent Applicant/Assignee:
HONEYWELL INC,
Inventor(s):
WOOD R Andrew,
RIDLEY Jeffrey A,
HIGASHI Robert E,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9950905 A1 19991007
Application: WO 99US6790 19990329 (PCT/WO US9906790)
Priority Application: US 9852630 19980331
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
CA JP AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: H01L-023/10
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 3496

English Abstract
A wafer-pair having at least one recess in one wafer forms at least one chamber with the attaching of the other wafer which has at least one port which is plugged with a deposited layer on its external surface. The deposition of the layer may be performed in a very low pressure environment, thus assuring the same kind of environment in the sealed chamber. The chamber may enclose at least one device such as a thermoelectric sensor, bolometer, emitter or other kind of device. The wafer-pair typically will have numerous chambers, and may be divided into chips.

23/5/3 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT


00519561 **Image available**
A METHOD OF MAKING A WAFER-PAIR HAVING SEALED CHAMBERS
PROCEDE DE PRODUCTION D'UNE PAIRE DE TRANCHES POSSEDANT DES ENCEINTES CLOSES
Patent Applicant/Assignee:
HONEYWELL INC,
Inventor(s):
WOOD R Andrew,
RIDLEY Jeffrey A,
HIGASHI Robert E,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9950913 A1 19991007
Application: WO 99US6890 19990330 (PCT/WO US9906890)
Priority Application: US 9852645 19980331
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
CA JP AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: H01L-027/16
International Patent Class: G01J-005/20
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 4243

English Abstract
A method for fabricating a wafer-pair having at least one recess in one wafer and the recess formed into a chamber with the attaching of the other wafer which has a port plugged with a deposited layer on its external surface. The deposition of the layer may be performed in a very low pressure environment, thus assuring the same kind of environment in the sealed chamber. The chamber may enclose at least one device such as a thermoelectric sensor, bolometer, emitter or other kind of device. The wafer-pair typically will have numerous chambers, with devices, respectively, and may be divided into a multiplicity of chips.